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Performance Analysis for Various Flip Flops using Topological Method for Power Saving

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Abstract

An extremely low-power flip-flop named topologically-compressed flip-flop is planned. As compared with standard FFs, the FF reduces power dissipation by seventy fifth at 1/3 information activity. This power reduction magnitude relation is that the highest among FFs that are reported thus far. The reduction is achieved by applying topological compression methodology, merger of logically equivalent transistors to associate unconventional latch structure. The terribly little variety of transistors, only three, connected to clock signal reduces the facility drastically, and therefore the smaller total transistor count assures identical cell space as standard FFs. In addition, absolutely static full-swing operation makes the cell tolerant of provide voltage and input slew variation. Associate experimental chip design with forty nm CMOS technology shows that nearly all standard FFs are replaceable with planned FF whereas protective the same system performance and layout space.

Keywords: *Flip-flops, low-power, VLSI.*

I. INTRODUCTION

Low power consumption has become a highly important design concern in this era and will become more and more important as we move to all mobile computing and communications. The transistor density of IC is growing at Moore's law rate and the incomparable battery advances will mandate low power methodologies and designs. In addition to the conventional mobile phone, digital camera, and tablet PC, development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. In those kinds of battery-working equipment, reduction of power is a very important issue, and demand for power reduction in LSI is increasing. In LSI, random logic contributes to more than half of the power is dissipated out of which 50% is dissipated by flip-flops (FFs). Many low-power FFs have been rushed into development in recent years. The conventional FF is still used in actual chip design, very often as a preferred FF because of its well-balanced power, performance and cell area. The purpose of this paper is to present a solution to achieve all of the goals: power reduction without any degradation of timing performance and cell area. In Section II, we review existing low-power FFs. In Section III, we show our design approach. In Section IV, we propose FF realization with a new methodology. In Section V, the detailed power and performance characteristics are shown compared to other FFs.

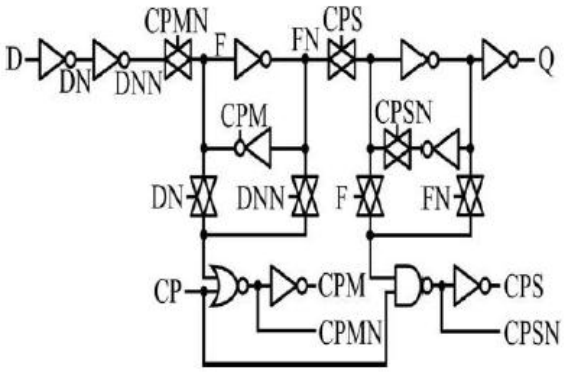

Fig.1. Conventional sense-amplifier flip-flop

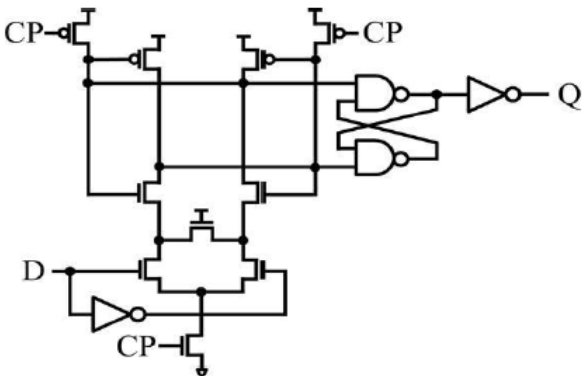

Fig.2. Differential sense-amplifier flip-flop (DiffFF)

II. RELATED WORK

In this section, we tend to analyze issues on antecedently reported typical low power FFs with comparison to a traditional FF shown in Fig. 1. A pair of shows a typical circuit of differential sense-amplifier type FF (Diff FF). This kind of circuit is extremely effective to amplify small-swing signals, therefore is usually utilized in output of memory circuits. In this FF, however, the result of power reduction goes down within the condition of lower information activity, because these varieties of circuits have pre-charge operation in each clock-low state. Moreover, if we tend to use reduced clock swing, a customized clock generator and an additional bias circuit are necessary. Fig.3 shows a circuit of conditional clocking kind FF (CCFF).

This circuit is achieved from a useful purpose of read. The circuit monitors input file amendment in each clock cycle and disables the operation of internal clock if input file aren't modified. By this operation, power is reduced once input file aren't modified. However sadly, its cell space becomes virtually double that of the standard circuit shown in Fig.4.

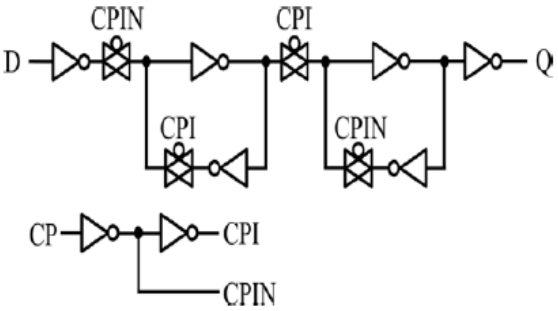

Fig.3. Conditional-clocking flip-flop (CCFF)

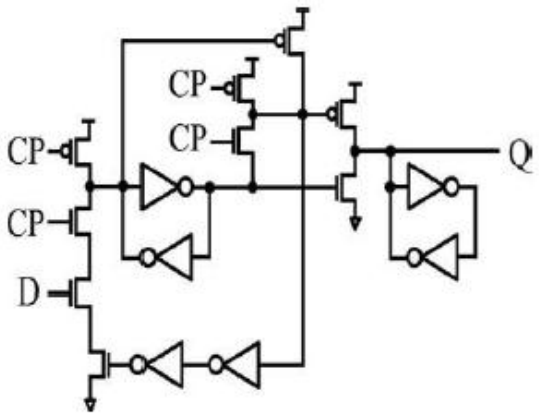

Fig.4. Cross-charge control flip-flop (XCFF)

Chiefly attributable to this size issue, it becomes arduous to use if the logic space is comparatively giant within the chip. Fig.4 four shows the circuit of cross-charge management FF (XCFF). The feature of this circuit is to drive output transistors separately so as to scale back charged and discharged gate capacitance. As a result, the impact of power reduction can decrease. Circuits as well as preset operation have an equivalent drawback. The adaptive coupling sort FF (ACFF), shown in Fig 4, is predicated on a 6-transistor memory cell. During this circuit, rather than the unremarkably used double channel transmission-gate, a single- channel transmission-gate with further dynamic circuit has been used for the information line so as to scale back clock related transistor count.

However, during this circuit, delay is well full of input clock slew variation as a result of differing kinds of single-channel transmission-gates area unit employed in an equivalent information line and connected to an equivalent clock signal.

Moreover, characteristics of monaural transmission-gate circuits and dynamic circuit's area unit powerfully full of method variation. Thus, their optimization is comparatively tough, and performance degradation across varied method corners may be a concern. Let us summarize the analysis on antecedently rumored low power FFs. For Diff FF and XCFF, pre-charge operation may be a concern particularly in lower information activity. As regards CCFF, its cell space becomes a bottleneck to use.

III. PROPOSED DESIGN APPROACH

In order to cut back the facility of the FF whereas keeping competitive performance and similar cell space, we have a tendency to tried to cut back the semiconductor unit count, particularly those operational with clock signals, while not introducing any dynamic or pre-charge circuit. The facility of the FF is usually dissipated within the operation of clock-related transistors, and reduction of semiconductor unit count is effective to avoid cell space increase and to cut back load capacitance in internal nodes. One reason is as a result of transmission gates would like a 2-phase clock signal, so the clock driver can't be eliminated. Another excuse is that transmission-gates ought to be created by each PMOS and NMOS to avoid degradation of information transfer characteristics caused by mono MOS usage. Therefore, rather than transmission-gate sort circuit, we have a tendency to begin with a combinable sort circuit as shown in Fig. 3. To cut back the transistor-count supported logical equivalence, we have a tendency to take into account a technique consisting of the subsequent 2 steps. Because the beginning, we have a tendency to attempt to have a circuit with or additional logically equivalent AND OR logic components that have identical signaling combination, particularly as well as clock signal because the input signals. Then, merge those components in semiconductor unit level because the second step.

IV. PROPOSED TOPOLOGICALLY-COMPRESSED FLIP-FLOP

A. Proposed FF and Transistor Level Compression

After investigating many kinds of latch circuits, we have set up an unconventionally structured FF, shown in Fig. 5. This FF consists of different types of latches in the master and the slave parts. The slave-latch is a well-known Reset-Set (RS) type, but the master-latch is an asymmetrical single data-input type. The feature of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Fig. 8 shows the transistor-level schematic of Fig. 7. Based on this schematic, logically equivalent transistors are merged as follows. For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 6 can

be shared as shown in Fig. 7. When either N3 or CP is Low, the shared common node becomes VDD voltage level, and N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP.

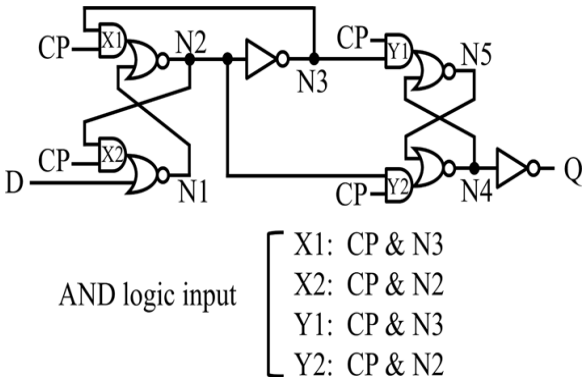

Fig. 5. Schematic diagram of proposed FF.

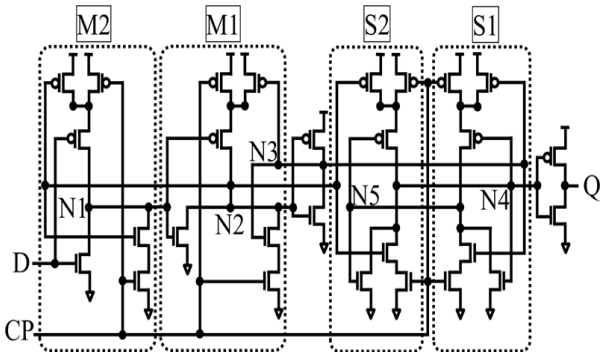

Fig. 6. Transistor level schematic of Fig. 7.

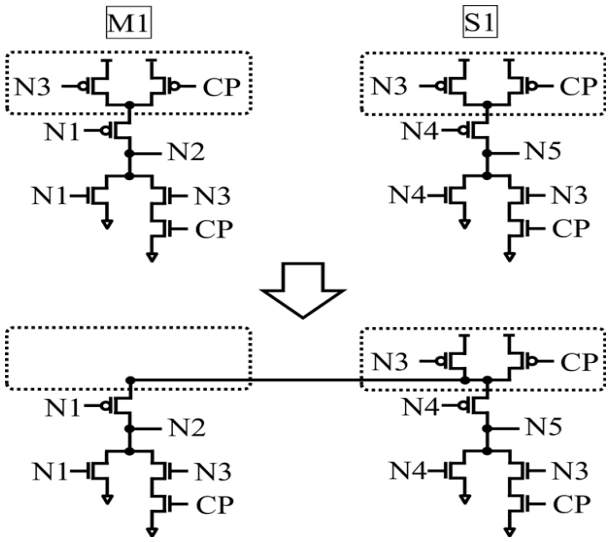

Fig. 7. Transistor merging in PMOS side.

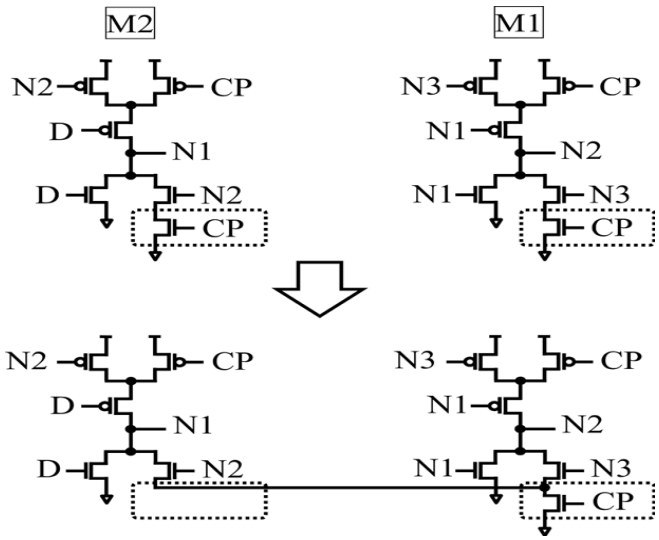

Fig. 8. Transistor merging in NMOS side.

and S2 blocks are shared. For the NMOS side, transistors of logically equivalent operation can be shared as well. Two transistors in M1 and M2 blocks in Fig. 10 can be shared. Transistors in S1 and S2 are shared as well.

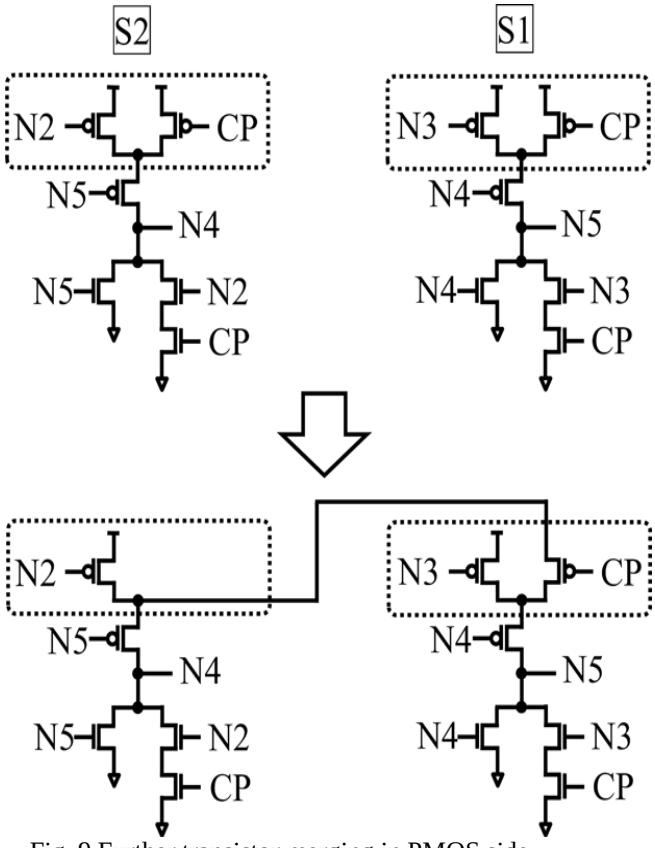

Fig. 9 Further transistor merging in PMOS side.

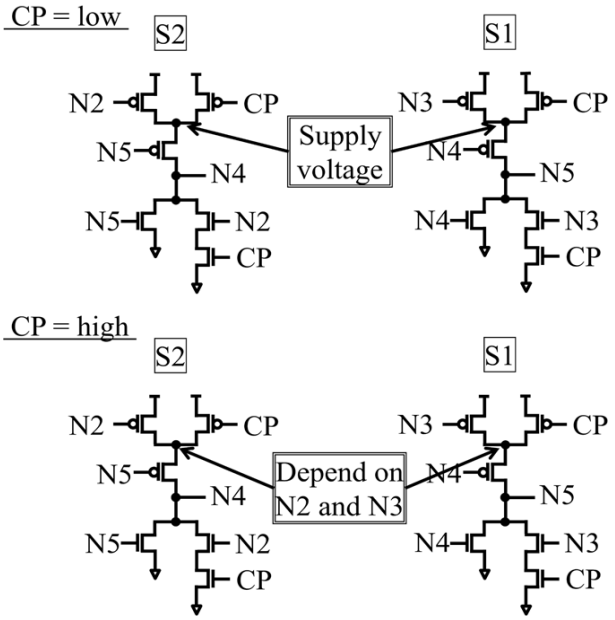

Fig. 10 The state of internal nodes.

Further in the PMOS side, CP-input transistors in S1 and S2, shown in Fig. 9, can be merged, because N2 and N3 are logically inverted to each other. When CP is Low, both nodes are in VDD voltage level, and either N2 or N3 is ON. When CP is High, each node is in independent voltage level as shown in Fig. 10. In consideration of this behavior, the CP-input transistors are shared and connected as shown in Fig. 9. The CP-input transistor is working as a switch to connect S1 and S2. This process leads to the circuit shown in Fig. 11. This circuit consists of seven fewer transistors than the original circuit shown in Fig. 6. The number of clock-related transistors is only three. Note that there is no dynamic circuit or pre-charge circuit, thus, no extra power dissipation emerges. We call this reduction method Topological Compression (TC) method. The FF, TC-Method applied, is called Topologically-Compressed Flip-Flop (TCFF).

B. Cell Operation

Fig. 12 shows simulation waveforms of the circuit shown in Fig. 11. In Fig. 11, when CP is low, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both VD1 and VD2 are pulled up to power-supply level, and the input data from D is stored in the master latch.

When CP is high, the PMOS transistor connected to CP turns

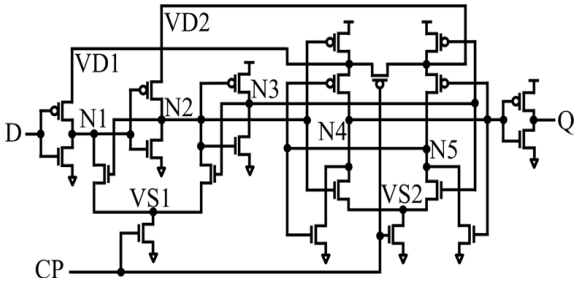

Fig 11.Transistor level schematic of topologically-compressed flip-flop (TCFF).

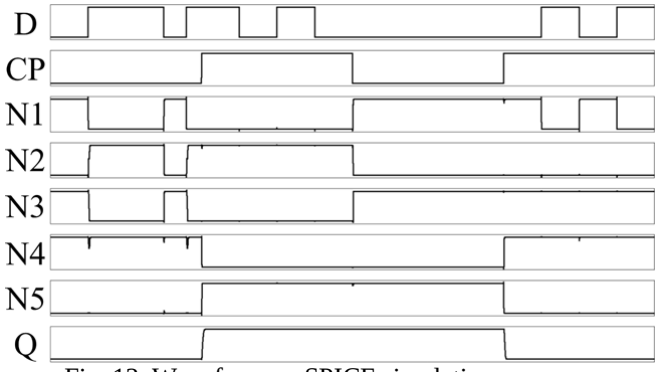

Fig. 12. Waveform on SPICE simulation.

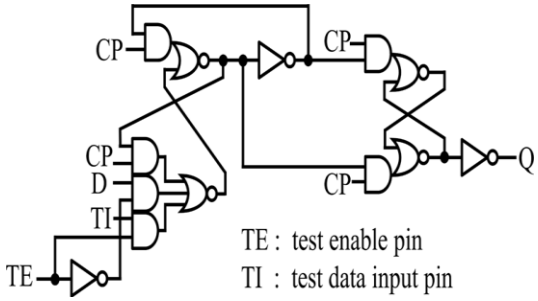

Fig. 13. TCFF with scan type.

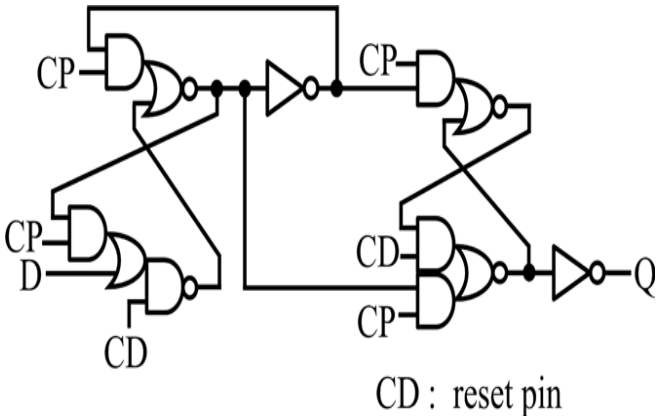

Fig. 14. TCFF with reset type.

off, the NMOS transistor connected to CP turns on, and the slave latch becomes the data output mode. In this condition, the data in the master latch is transferred to the slave latch, and then outputted to Q. In this operation, all nodes are fully static and full-swing. The current from the power supply does not flow into the master and the slave latch simultaneously because the master latch and the slave latch become active alternately. Therefore, timing degradation is small on cell performance even though many transistors are shared with no increase in transistor size.

C. Cell Variation

LSI designs require FFs having additional functions like scan, reset, and set. The performance and cell area for these cells are also important. TCFF easily realizes these cells with less transistor-count than conventional FFs. The circuit diagrams of TCFF with scan, reset, and set are

shown in Figs. 13–15. Each circuit can be designed with similar structure, and these FFs also have three transistors connected to CP so the power dissipation is nearly the same as that of TCFF. Detailed characteristics are

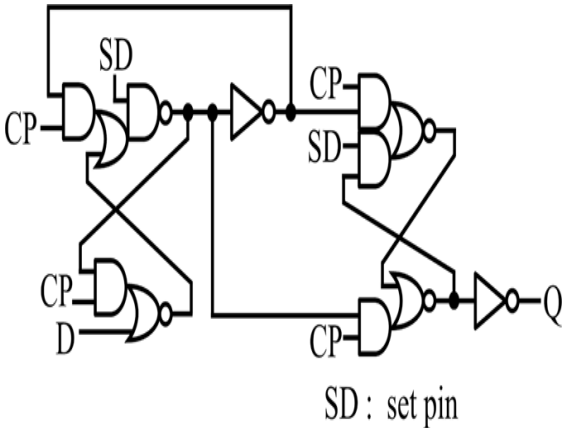

Fig. 15. TCFF with set type.

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V. PERFORMANCE SIMULATION

The performance of TCFF is demonstrated by SPICE simulation with 40 nm CMOS technology. For comparison with other FFs, the same transistor size is applied for every transistor in each FF including TCFF in order to simulate the same conditions. Some standard values are assumed for transistor sizes for the purpose of comparison; 0.24 m for width and 0.04 m for length in PMOS, and 0.12 m for width and 0.04 m for length in NMOS.

Fig.16 shows the normalized power dissipation versus data activity compared to other FFs. TCFF consumes the least power among them in almost all ranges of data activity. Average data activity of FFs in an LSI is typically between 5% and 15%. The power dissipation of TCFF is 66% lower than that of TGFF at 10% data activity. In the same way at 0% data activity, it is 75% lower. Table I summarizes the transistor-count, the CP-Q delay, the setup/hold time, and the power ratio of each FF. As for delay, TCFF is almost the same as the conventional FF, and better than other FFs. Setup time is the only inferior parameter to the conventional FF, and about 70 ps larger than the value of the conventional one. For hold time, TCFF is better than the conventional FF. In summary, only setup time is large, but TCFF keeps competitive performance to the conventional and other FFs.

Fig.17 shows the supply-voltage dependence of the CP-Q delay. TCFF is possible to operate down to 0.6 V supply voltage due to essentially fully-static function. Though TCFF operates with single phase clock signal, a clock buffer is not necessary. The circuit is directly driven from a clock pin. Fig. 20 shows the clock-input-slew dependence of the CP-Q delay. ACFF has more clock-input-slew dependence compared to other FFs, thus it becomes difficult to use in large input transition time. The characteristics of TCFF are stable and the second best following TGFF.

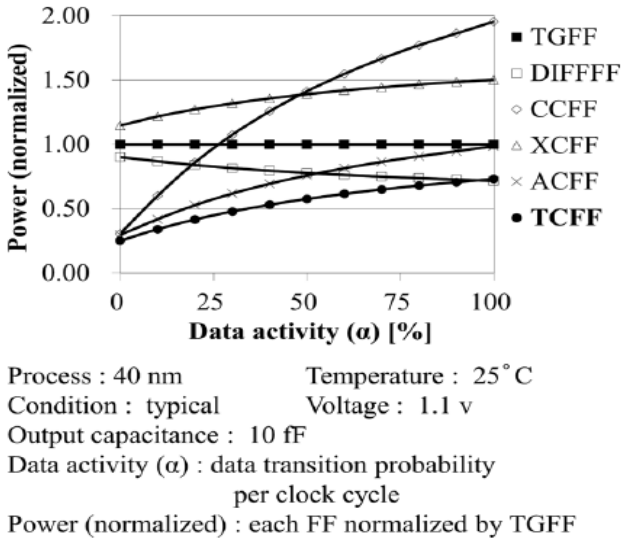

Fig.16. Power simulation results of TCFF and other FFs

TABLE I: PERFORMANCE COMPARISON OF TCFF AND OTHER FFS

S.No	Conventional FF	TCFF	TGFF
Power in mW	183	148	129
Supply Voltage	0.9	0.9	0.9
Frequency in MHz	330	330	330
Propagation Delay in ns	203	186	178
Area (mm^2)	0.0998	0.0094	0.067

Table 1.Comparison of various FF

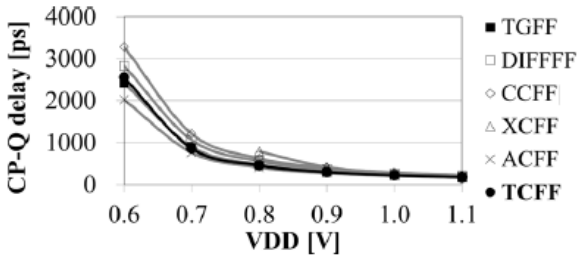

Fig.17. Supply voltage dependency

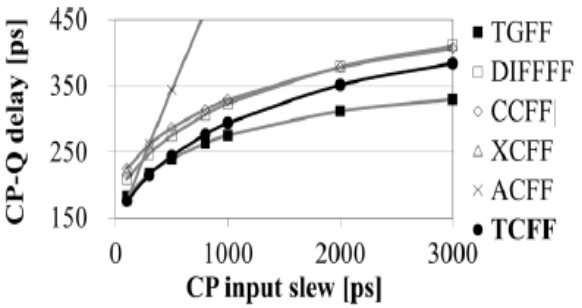

Fig.18. Input slew dependency

Fig. 17 shows the normalized power versus the data activity for six varieties of TCFF including the basic type, and Table II shows performances of various TCFFs in the same conditions as Table I. Every cell inherits the strength of the original TCFF cell structure. No difference is observed among cell variations.

Fig.18 shows the layout of TGFF and TCFF with scan. Because TCFF needs more wiring resources for master and slave latch in the layout, it uses metal3 as compared to TGFF using up to metal2. But because the number of transistors in TCFF is fewer than the TGFFs, TCFF can be realized in slightly smaller cell area than the conventional one. In this layout, the area is adjusted to grid base design, resulting in the same area as the conventional one. Thus, it is easy to replace the conventional FF with TCFF if the cell replacement process is executed after pre-layout and timing analysis. In this section, TCFF's lowest power dissipation, competitive performance, and cell area are explained. In the next section, how effectively TCFF is applied to actual chip design is shown by placement and routing experiment.

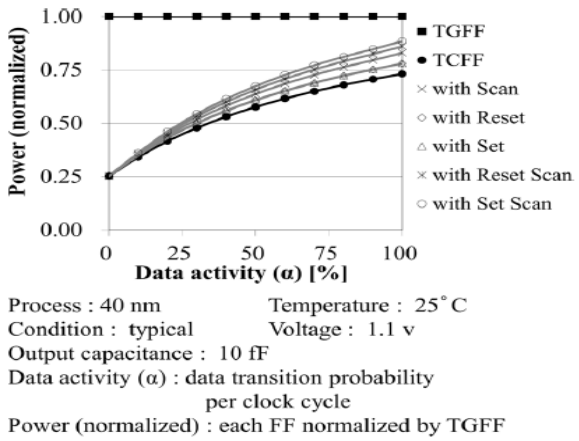

Fig.19. Power simulation results of various TCFFs

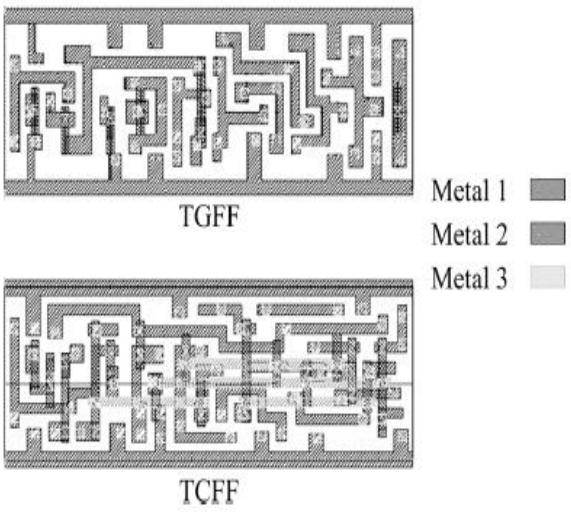

Fig.20. The cell layout with scan

VI. CONCLUSION

An extremely low-power FF, TCFF, is planned with topological compression style methodology. TCFF has very cheap power dissipation in most vary of the information activity compared with alternative low-power FFs. the facility dissipation of TCFF is 80 % not up to that of TGFF at third information activity while not space overhead. The topology of TCFF is definitely expandable to varied sorts of FFs while not performance penalty. Applying to a 250 MHz experimental chip style with forty nm CMOS technology, ninety eight of standard FFs area unit replaced by TCFFs. in an exceedingly whole chip,37% of power reduction is calculable with very little overhead of space and temporal arrangement performance.

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